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09/221,291	12/23/1998	MARTIN H. GRAHAM	003921.P005	4813

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EXAMINER

BURD, KEVIN MICHAEL

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2631

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/221,291
Filing Date: December 23, 1998
Appellant(s): GRAHAM, MARTIN H.

MAILED

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GROUP 2600

Edwin Taylor
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12/21/2005 appealing from the Office action mailed 3/18/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

5,999,848	GORD et al	12-7-1999
5,654,978	VANDERPOOL et al	8-5-1997

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

- I. Claims 19-25 are rejected under 35 U.S.C. 103(a)

The rejections are hereby reproduced for convenience.

I. Claims 19-22, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gord et al (US 5,999,848) in view of Vanderpool et al (US 5,654,978).

Regarding claims 19 and 25, Gord discloses a method of encoding a signal shown in figures 6 and 8. A first biphasic pulse has a first portion of a first polarity and a second portion of a second polarity. Following the first pulse, a waiting period where no information is sent occurs. After the waiting period, a second biphasic pulse is transmitted, having two portions, one with a first polarity and one with a second polarity. The time periods and amplitudes are also shown in figure 6. The biphasic pulse transmission is described in column 16, lines 25-43. Gord does not disclose the duration of the waiting a time period being selected to represent a plurality of data bits. Vanderpool teaches a method of encoding information in a pulse position modulation system. A time delay between a first pulse and a second pulse is used to encode data. For example, a short time delay between the first and second pulses may indicate a logical "0", while a longer delay may be used to encode a logical "1" as stated in claim 1, lines 10-18. The delays can represent a plurality of data bits (column 3, lines 8-17 and column 5, lines 37-40). Figures 2-4 show the pulses are detected at a time after the first pulse is transmitted. Figure 4 shows the use of biphasic pulses in the transmission system. It would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the pulse position modulation system for encoding additional

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data bits as stated by Vanderpool into the system of Gord. Each possible choice, for the data pulse, of delay time and transmission code may represent a separate set of multiple data bits (column 2, lines 3-5). Therefore, more information can be transmitted than before during the same transmission period.

Regarding claim 20, the biphasic pulse has no DC component since the positive amplitude is equal to the negative amplitude.

Regarding claim 21, the amplitude and pulse width of the pulses are shown in figure 6 of Gord.

Regarding claim 22, figure 6 of Gord shows the biphasic pulse is encoded. One amplitude represents a "1" bit while a second amplitude represents a "0" bit.

Regarding claim 24, the combination of Gord and Vanderpool discloses a method for encoding a signal above. The combination does not disclose the transmission occurs over a twisted wire pair. However, Gord discloses the transmission occurs over a wire transmission system in column 16, lines 16-24. It would have been obvious for one of ordinary skill in the art at the time of the invention transmit the signals generated by the combination in any conventional wired transmission system that allows the information to be received at the desired location free of interference.

II. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gord et al (US 5,999,848) in view of Vanderpool et al (US 5,654,978) further in view of Pernyeszi (US 5,969,547).

Regarding claim 23, the combination of Gord and Vanderpool discloses a method for encoding a signal stated in paragraph 3. The combination does not disclose the pulse width of each of the pulses represents at least one bit. Pernyeszi discloses pulse widths carry the information with a pulse's width representing a digital value (column 1, lines 17-25). It would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate Pernyeszi's method of pulse width encoding data into the method of the combination of Gord and Vanderpool to transmit more information than either system is capable alone. Information can be transmitted over less time and the transmitter will consume less power due to the limited transmission time.

(10) Response to Argument

A. Claims 19-22, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gord et al (US 5,999,848) in view of Vanderpool et al (US 5,654,978).

Appellant submits Gord generates first and second biphasic pulses but the biphasic pulses do not alternate. Appellant points to figure 6 of Gord to illustrate this point. However, figure 8 of Gord shows the generation of biphasic pulses with alternating polarity. Gord discloses a first biphasic pulse having a first portion of a first polarity (the positive component of the INPUT DATA "1" pulse) and a second portion of a second polarity (the negative component of the INPUT DATA "1" pulse). Following the

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first pulse, a waiting period where no information is sent occurs (the time period between the INPUT DATA "1" biphasic pulse and the INPUT DATA "0" biphasic pulse). After the waiting period, a second biphasic pulse is transmitted having a third portion of the second polarity (the negative component of the INPUT DATA "0" pulse) and a fourth portion with the first polarity (the positive component of the INPUT DATA "0" pulse). Data is encoded on these pulses. Gord states in column 16, lines 35-43, "a binary '1' may be represented by a biphasic pulse of one phase, e.g., a positive current pulse followed by a negative current pulse; while a binary '0' may be represented by a biphasic pulse of the opposite phase, e.g., a negative pulse followed by a positive pulse."

Appellant submits Vanderpool transmits data by the duration or dead time between the pulse frames 204 and 205 in figure 4. Appellant concedes that this is what is being done in the present invention, except for the fact that the pulses are not alternating biphasic pulses required by the claims in page 5 of the appeal brief.

Appellant states there is no teaching in either reference for taking the biphasic pulses of Gord and placing them into Vanderpool. However, this is not what was done in the rejection of the claims. After a description of Gord, the rejection of the claims state:

Gord does not disclose the duration of the waiting a time period being selected to represent a plurality of data bits. Vanderpool teaches a method of encoding information in a pulse position modulation system. A time delay between a first pulse and a second pulse is used to encode data. For example, a short time delay between the first and second pulses may indicate a logical "0", while a longer delay may be used to encode a logical "1" as stated in claim 1, lines 10-18. The delays can represent a plurality of data bits (column 3, lines 8-17 and column 5, lines

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37-40). Figures 2-4 show the pulses are detected at a time after the first pulse is transmitted.

Figure 4 shows the use of biphasic pulses in the transmission system. It would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the pulse position modulation system for encoding additional data bits as stated by Vanderpool into the system of Gord. Each possible choice, for the data pulse, of delay time and transmission code may represent a separate set of multiple data bits (column 2, lines 3-5). Therefore, more information can be transmitted than before during the same transmission period.

Therefore, the method of encoding information between biphasic pulses of Vanderpool is incorporated into the pulse generating method of Gord is the combination stated in the previous rejection not the combination disclosed by Appellant on page 5 of the appeal brief.

Appellant, also, states, the combination would require Gord to transmit a sequence of 1010101010. This is not entirely correct. If the combination of Gord and Vanderpool were to transmit the sequence of 101010101010 (with, of course, data encoded in the time period between the biphasic pulses) the limitations of the claims would be met. However, simpler data sequences also meet all of the claim limitations. Examples of sequences that will satisfy the claim limitations are any sequence of bits that includes a biphasic "1" followed by a biphasic "0" or a biphasic "0" followed by a biphasic "1". The claims recite the limitation of one biphasic pulse followed by a second biphasic pulse of opposite polarity. The pending claims only claim these two pulses. The preceding pulses and the subsequent pulses are not claimed. For this reason, the examiner disagrees with the statement on page 5 of the appeal brief stating "this would require, in terms of Gord, that Gord transmits 1010101010."


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(11) Related Proceeding(s) Appendix


No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,


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